VLSI Test Workshop

Event Schedule & Venue

18th to 20th April 2025

09:00AM to 05:00PM

BITS-Pilani, Hyderabad Campus

Organized by

BITS-Pilani,

Hyderabad Campus

Department of EEE

IEEE COMPUTER SOCIETY TTTC Test Technology Technical Community

About Workshop

VLSI Test Workshop provides a comprehensive examination of advanced design-for-test (DFT) methodologies and essential testing techniques for contemporary VLSI systems. Participants will explore topics such as scan-based testing, memory testing, and fault modeling, gaining insights into enhancing testability and fault detection. The workshop features presentations from industry leaders, career development sessions, and hands-on laboratory experiences with cutting-edge testing tools. Additionally, attendees will have valuable networking opportunities to connect with professionals and researchers, making this event ideal for anyone seeking to deepen their knowledge in VLSI testing and semiconductor design.

Who can attend?

Workshop invites B.Tech students from 3rd year onwards, as well as master's students, research scholars, faculty, and industry professionals keen on enhancing their understanding of VLSI testing methodologies and DFT techniques. Participants will have the opportunity to explore scan-based testing, memory testing, fault diagnosis, and industry standards in a collaborative environment. This Workshop is ideal for those seeking practical insights, engaging in hands-on sessions, and connecting with experts who are leading advancements in VLSI design and testing.

Prerequisites: A foundational knowledge of digital design is required. Familiarity with Unix or Linux is desirable but not mandatory. Knowledge of Verilog or VHDL is a plus.

About EEE Department

The Department of Electrical and Electronics Engineering at BITS Pilani, Hyderabad campus has been operational since 2008, offering B.E. programs in ECE, EEE, and EIE, and M.E. in Communication Engineering, Microelectronics Engineering, Embedded Systems, along with doctoral programs. It boasts extensive laboratory and infrastructural teaching, training, and research facilities.

About BITS

Birla Institute of Technology & Science Pilani (BITS-Pilani) is an institution of international repute. Over the years, BITS-Pilani has provided the highest quality technical education to students from all over India and abroad admitted on the basis of merit. BITS-Pilani is ranked among the top engineering institutes of India. BITS is a multi- locational university with four campuses in India, at Pilani, Goa, Hyderabad, Mumbai and one international campus in Dubai (UAE). During its five decades of existence as a university, BITS- Pilani has established strong linkages with industries, R&D organizations and financial institutions through its university-industry linkage programs.

Important Dates

Registration begins	**: 25th March 2025**
Registration ends	**: 15th April 2025**

Registration

BE/ME Students	**: 944 (800 + 18% GST)**
PhD/Project Scholars	**: 1416 (1200 + 18% GST)**
Faculty Members	**: 1770 (1500 + 18% GST)**
Industry Professionals	**: 2124 (1800 + 18% GST)**

Includes Registration Kit, Participation Certificate, Refreshment & Lunch. Limited seats based on First Come First Serve basis. Accommodation in student hostels to limited participants, subject to availability, on a paid basis.

Every participant of the workshop will receive a certificate from the organizers.

Resource Persons

Venkata Rangam Totakura

Senior Director

Infineon Technologies

Rajit Karmakar

Member of Technical Staff

AMD

Bharath Nandakumar

R&D Manager

Cadence Design Systems

Sameer Chillarige

R&D Director

Cadence

Prasad Mantri

Distinguished Engineer

Eximietas Design

Payment Details

https://pmny.in/elZlwOL21NAt

Registration Details

https://forms.gle/ueQTgRK5CUGbDCfU6

Note: **Kindly complete the payment first and then upload the payment details in the registration form.**

Agenda

18th April 2025 Friday

Day 1

09:00AM - 09:30AM Inauguration and Introduction
09:30AM - 10:30AM Introduction to Design for Test-1
10:30AM - 11:00AM Networking over Tea/Coffee
11:00AM - 12:30PM Introduction to Design for Test-2
12:30PM - 01:30PM Networking over Lunch
01:30PM - 02:45PM Fault models
02:45PM - 03:00PM Networking over Tea/Coffee
03:00PM - 04:00PM Fault Simulation and Test Generation
04:00PM - 05:00PM DFT as a career

19th April 2025 Saturday

Day 2

09:00AM - 10:30AM Scan Based Testing
10:30AM - 11.00AM Networking over Tea/Coffee
11.00AM - 12:30PM Scan Compression & Logic BIST
12:30PM - 01:30PM Networking over Lunch
01:30PM - 02:30PM Test Diagnosis
02:30PM - 02:45PM Networking over Tea/Coffee
02:45PM - 03:45PM Memory Testing
03.45PM - 05:00PM Test Standards

20th April 2025 Sunday

Day 3

09:00AM - 10:30AM Lab session - 1
10:30AM - 10.45AM Networking over Tea/Coffee
10.45AM - 12:30PM Lab Session – 2
12:30PM - 01:30PM Networking over Lunch
01:30PM - 02:00PM Open house and conclusion
02:00PM - 03:30PM Lab session – 3
03:30PM - 03:45PM Networking over Tea/Coffee

For any queries, contact

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