## Timeline

**Registration Deadline**

20 Feb 2026

**Round 1 submission**

15 March 2026

**Round 1 result**

20 March 2026

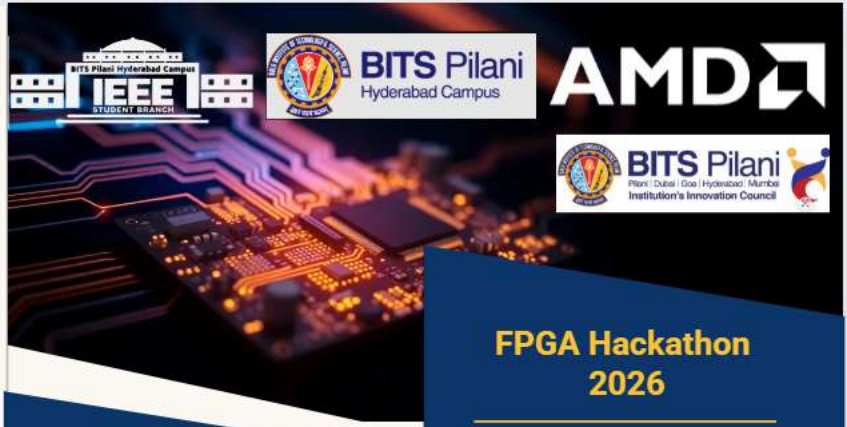
**Round 2 Hackathon**

10 - 11 April 2026

## Sponsorship & Organization

Faculty: Prof. Amit Kumar Panda
AMD: Mr. Santosh Yachareni
Student Coordinator: Sharundhathya C, IEEE Student Branch
Student Co-Coordinator: Sree Harsha G, IEEE Student Branch

Sponsored by **AMD** &
Co-Sponsored by ***IIC, BITS Pilani Hyderabad***




## Key Focus Areas

**AMD/Xilinx FPGA**
Leverage AMD/Xilinx architectures to achieve maximum throughput and energy efficiency for real-time intelligence.

**Real-time performance**
Achieve maximum processing speed and low latency for real-time applications.

**Efficient hardware utilization**
Maximize the use of FPGA resources to create compact and powerful solutions.

# FPGA Hackathon 2026

₹ Up to 1.5 Lakh Prize Pool

- Progress from an Online Screening to an Offline Grand Finale at BITS Pilani, Hyderabad Campus
- Compete for a **₹1.5 Lakhs prize pool** with **no entry fee**
- Network with experts and gain national-level visibility.

## About the **Hackathon**

### Round 1

Participating teams must choose a real-world application and develop a robust AI/ML model using software tools like Python, MATLAB, or C/C++. This stage focuses on implementing the inference engine in Verilog RTL as a dedicated hardware accelerator, validated through simulation or FPGA prototyping. Submissions will be evaluated on technical complexity, novelty, and the ability to demonstrate efficient hardware utilization for real-time edge performance.

### Round 2

**Day 1 – On-site Hackathon**
Finalist teams will take on the grand innovation challenge, deploying the inference stage of their Edge AI models at the RTL level using real-time data and sensor interfacing on AMD/Xilinx FPGA platforms. Includes bonus sessions with expert talks and a hands-on workshop on hardware-accelerated Edge AI.

**Day 2 – Presentations & Outreach**
Features technical presentations, poster sessions, expert talks, live demos, and the final results announcement.

## Participation

**Team Size:** 2 members per team
**Eligibility:** BE, ME, MSc, and PhD students from all institutions across India
**Zero Entry Fee**
**Travel reimbursement:** Coverage of up to **₹3,000 per student** for both team members selected for Round 2
**Poster presentation:** Submissions for round 1 will also be considered for a poster presentation

## Up to 1.5 Lakh Prize Pool

## Application **Domains**

### Traffic Management System:

Edge AI facilitates localized, real-time decision-making to reduce congestion and pollution

### Smart Energy System

Intelligent, on-device resource optimization for buildings and grids without relying on the cloud

### Agriculture

Edge AI for smart farming — crop disease detection, soil moisture classification, and yield prediction.

### Biomedical Systems

Real-time health monitoring — ECG/EEG anomaly detection, heart rate analysis, and medical image classification.

### Defense Systems

Mission-critical intelligence — target detection, anomaly detection in radar/sonar, and multi-sensor data fusion.

## Submission & Evaluation

Complete Verilog RTL source code
5-10 minute video demo
Technical report covering the application, AI model, design, and novelty.


## Contact & Venue

BITS Pilani, Hyderabad Campus

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