Birla Institute of Technology & Science, Pilani
Hyderabad Campus

Dated: 11/02/2026

Applications are invited for the post of **Post-Doctoral Fellow (PDF)**

Project Title : **LLM-Driven RTL Design Tool for AMD FPGAs: A Targeted Approach**

Funding Agency : AMD

Project Location : BITS Pilani, Hyderabad Campus

Duration : 1 Years (12 Months)

Position: Post-Doctoral Fellow (PDF)

Fellowship: Rs. 80,000

Essential Qualification: PhD in CSE/ECE or related specializations

Desired Qualification: PhD in CSE/ECE or related specializations

Desired Expertise: Strong understanding of basic Machine Learning, Deep Learning or Reinforcement Learning, Strong understanding of Large Language Models Learning Algorithms, Proficiency in C, C++ or Python, Knowledge of Computer Systems/Computer Architecture.

Interested candidates should apply by filling out the form https://forms.gle/a1kaLc1s4eynE7DR9 and submit on or before **18.02.2026 (Wednesday).**

PI and Co-PI Details	**Paresh Saxena**, Associate Professor, Department of Computer Science & Information Systems && **Soumya J**, Associate Professor, Department of Electrical and Electronics Engineering **Phone:** 040-66303591/690 **Email:** psaxena@hyderabad.bits-pilani.ac.in,soumyaj@hyderabad.bits-pilani.ac.in **Website link:** https://www.bits-pilani.ac.in/hyderabad/dr-paresh-saxena/, https://www.bits-pilani.ac.in/hyderabad/soumya-j/

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