



Dated: 21/11/2025

Applications are invited for the post of **Junior Research Fellow (JRF)**

Project Title : AI/ML based Floorplanning for Dynamic Function Exchange (DFX) in FPGA Architectures

Funding Agency : AMD

Project Location : BITS Pilani, Hyderabad Campus

Duration : 1 Year (12 Months)

Position: Junior Research Fellow (JRF)

Fellowship: Rs. 37,000

Essential Qualification: B.E/B.Tech in ECE/CSE

Desired Qualification: M.E/M.Tech in Microelectronics and VLSI/Embedded Systems/CSE or related specializations.

Desired Expertise: Strong understanding of RTL Design
Knowledge of Computer Architecture
Proficiency in Verilog
Experience with UVM, Vivado Tool/Cadence Tools/Synopsys Tools
Candidates having strong expertise in working with Machine Learning and Large Language Models may also be considered

Interested candidates should apply by filling out the form <https://forms.gle/FM2mp3meBRx5ExDN9> and submit on or before **28.11.2025 (Friday)**

****Selected candidates shall get the additional opportunity to be enrolled for the Full-Time Ph.D program of BITS Pilani, Hyderabad Campus, based on the institutional rules and regulations.**

PI Details	Soumya J Associate Professor, Department of Electrical and Electronics Engineering Phone: 040-66303690 Email: soumyaj@hyderabad.bits-pilani.ac.in Website link: https://www.bits-pilani.ac.in/hyderabad/soumya-j/
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