

BIRLA INSTITUTE OF TECHNOLOGY AND SCIENCE, PILANI
I SEMESTER 2008-09
EEE/INSTR/CS C391 DIGITAL ELECTRONICS AND COMPUTER ORGANIZATION
COMPREHENSIVE EXAMINATION

MM: 120 Time: 3Hrs 12-12-2008

Note: The question paper consist of two parts PART A and PART B. PARTA to be answered in the question paper itself and PART B in a separate answer sheet provided. The expected time for completion of PART A is 1 Hr, however you can collect Part B question pa per once you submit Part A. You can use last two pages of Part B answer book for rough work.

Part A (CLOSED BOOK)

MM: 40

Name:

Sec No:

IDNO:

Marks Obtained:

Recheck request if any:

Q1. Represent the decimal number 43 in the following codes:

(i) Excess-3

(ii) 643-2

(iii) Gray

(3)

Q2. For the Boolean function $F(A,B,C,D) = m(0,4,7,8,10,14)$ and $d(2,5)$ write down the PIs and EPIs using K-Map . Also write the MSP for F.

PI =

EPI =

F =

(4)

Q3. Using Transmission Gates and Inverters implement the function $Y = A(B+CD)$.

(4)

Q4. The Pair of Boolean Functions $F1 (A,B,C,D) = m(2,4,5,10,12,13,14)$ and $F2 (A,B,C,D) = m(2,9,10,11,13,14,15)$ are to be realized with a PLA having only true outputs. Identify the minimum size PLA and draw the PLA Programming table. (5)

Q5 (i) Draw the excitation table of a JK Flip -flop.

(ii) What is setup time and hold time in D FF.

(2+2)

Q6. Implement the given expression using only two -input NAND gates. No gate should be used as a NOT gate. Assume that complements of inputs are available. (5)
 $F=B'C'D'+BD+ACD+ABC$

Q7.(i) What is the size of ROM required to implement a one digit BCD to GRAY code converter?

(ii) A Processor has 5124 different microinstructions and 256 different control signals. Of all the microinstructions only 1024 are unique. Calculate the amount of saving (in number of bits) which will result if the processor is implemented using nanomemory.

(2+3)

Q8. (i) What are the two disadvantages of a fully set associative cache?

(ii) Construct a 2-input LUT used in FPGA using 2:1 MUXs and storage cells.

(2+2)

Q9. Consider a machine with a byte addressable main memory of 2^{16} bytes and block size of 16 bytes. Assume that a direct mapped cache consisting of 64 lines is used with this machine.

(a) How is a 16-bit memory address divided into tag, line number and byte number?

(b) How is a 16-bit memory address divided if the mapping used is fully set associative?

(c) How is a 16-bit memory address divided if the mapping used is 4-way set associative?

(2+2+2)

Q1. Design a clocked sequential circuit that has one input B_i and one output B_o and a clock input CK. When the input becomes 1 (Logic high), the output should become 1 (Logic high) at the next rising edge of the clock and should stay high for only one clock period (Refer Fig. Q1). The operation is repeated whenever B_i becomes 0 and returns to 1 again. Design the circuit using minimum number of D Flip Flops and gates. (14)

Q2. Design a multiplier circuit that takes a 4-bit binary number as input and multiplies it by either 2, 4 or 16. The multiplication factor is decided by another two-bit input C1C0 according to the table given below:

C1C0	Multiplication Factor
00	2
01	4
10	16

The circuit should produce the output after inputs have been setup and an active high 'BEGIN' signal is applied. You may choose only from the following components for your design:

1. 3-bit binary UP counter with asynchronous CLEAR (active high) and active low ENABLE – 1 No.
2. 3:8 decoder with active high outputs and active high ENABLE – 1 No.
3. 4:1 MUX – 1 No.
4. 8-bit Shift register with asynchronous parallel load and parallel outputs – 1 No.
5. 2 input and 3 input AND gates and NOT gates.

(15)

Q3. Design a synchronous counter with irregular binary count sequence of 001 -010-101-111-001... You are given only the following components:

1. IC 7476 – 1 No.
2. IC 7432 – 1 No.
3. IC 7486 – 1 No.

(10)

PTO→

Q4.(i) Design a 2-bit equality comparator that takes two 2-bit binary numbers as input and produces logic high on output only if the two input numbers are equal. Use a 4:1 MUXs a 2: 4 Decoder (with active high outputs) only for your design. (7)

(ii) For a CPU with a single bus organization (ref text book) give the RTL statement and control sequence implementing the instruction RET . The RET instruction is used by the processor to return from procedure call. (6)

Q5. Design a circuit that implements the following function:

$SUM = [(X+2) \bmod 8] + Y$ where X and Y are two 3 bit binary numbers and SUM is a 4 bit binary output.

Use only the following components to make your design.

1. 3:8 Decoder with active high outputs and active high ENABLE
2. 8:3 Encoder with active high inputs, active high ENABLE
3. 3-bit binary adder

[Note: $(X+2) \bmod 8$ means $(X+2)$ divided by 8 with remainder as answer]

(13)

Q6. A circuit for checking the validity of a BCD input number is to be designed. The design (in data section) uses a 4-bit shift register, a 4-bit comparator and a D Flip flop along with other required gates. The shift register and D FF is cleared on the rising edge of first clock pulse and thereafter the BCD number to be checked is entered serially with every clock pulse into the shift register starting from L SB. On the next clock pulse the output of the D Flip Flop is then set to 1 if the number is valid BCD, else it is set to 0 and the circuit returns back to the initial state.

- (a) Draw the ASM chart for the above problem.
- (b) Do the controller design using one-hot state assignment.
- (c) Show the data section design.

(15)